Circuit design of ALU based on the Computer architecture book by Maurice Manu (Chapter 4).

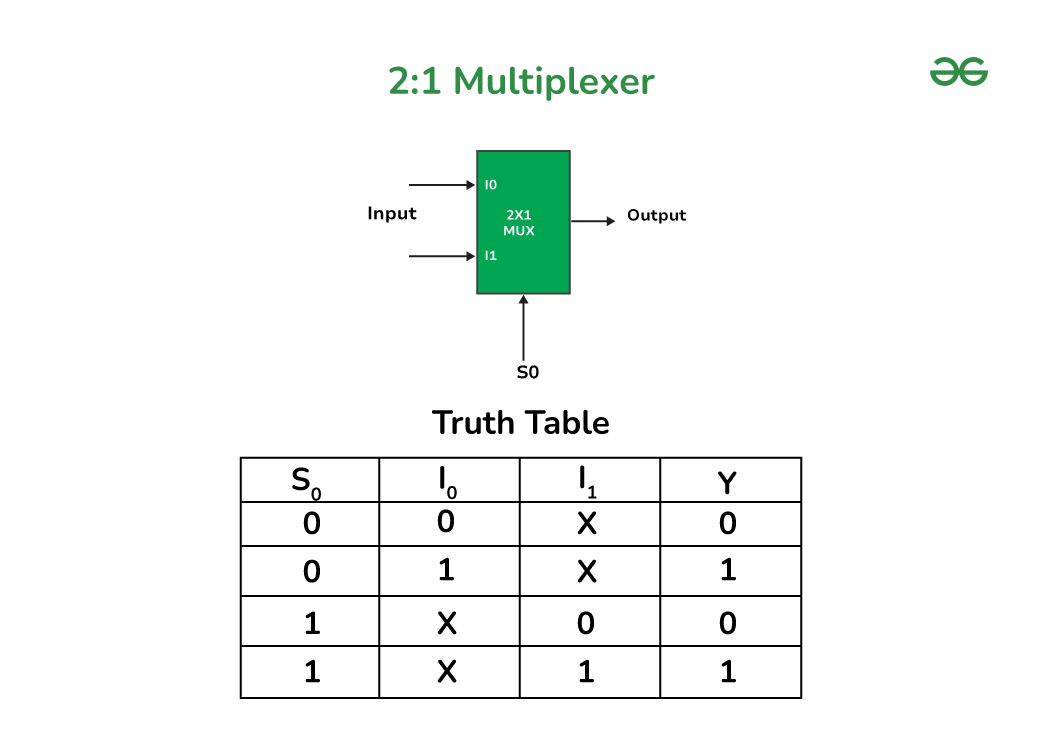
What is ALU?

In computing, an **arithmetic logic unit** (**ALU**) is a combinational digital circuit that performs arithmetic and bitwise operations on integer binary numbers.

Requirements for this circuit: Multiplexer (MUX), Full Adder(FA), Sheft Circuit ,gates(AND,OR,NOT,XOR,…).

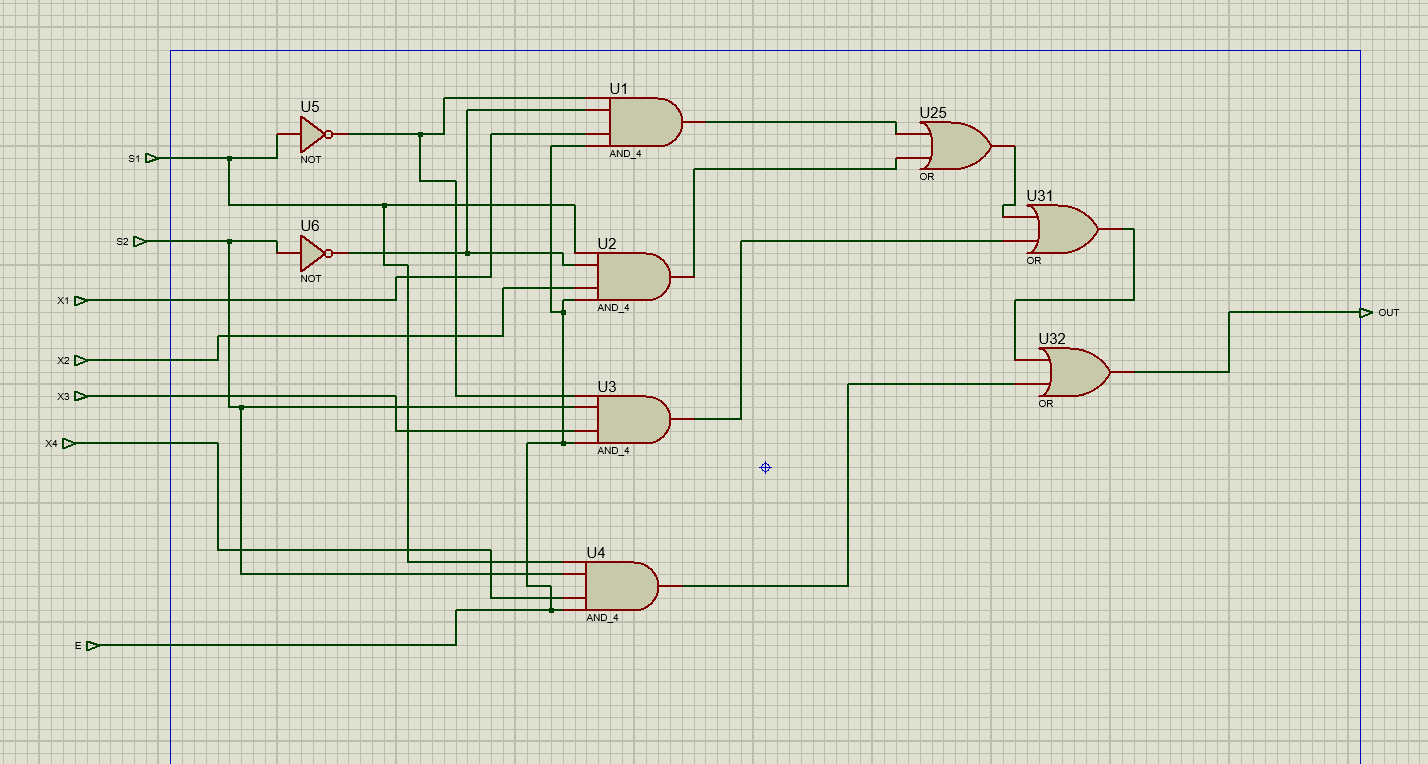
HOW TO MAKE MULTIPLEXER?

In fact, to build a MUX, you need to choose one of several different states. This can be done using logic gates.

Image from : .[geeksforgeeks.org](https://www.geeksforgeeks.org/multiplexers-in-digital-logic/)

To build a MUX you need AND,OR,NOT gates

In the figure below you see the circuit of a 4-to-1 MUX



HOW TO MAKE A FULL ADDER?

A full adder is made by connecting two half adders. To build a half-adder circuit we need AND,XOR gates

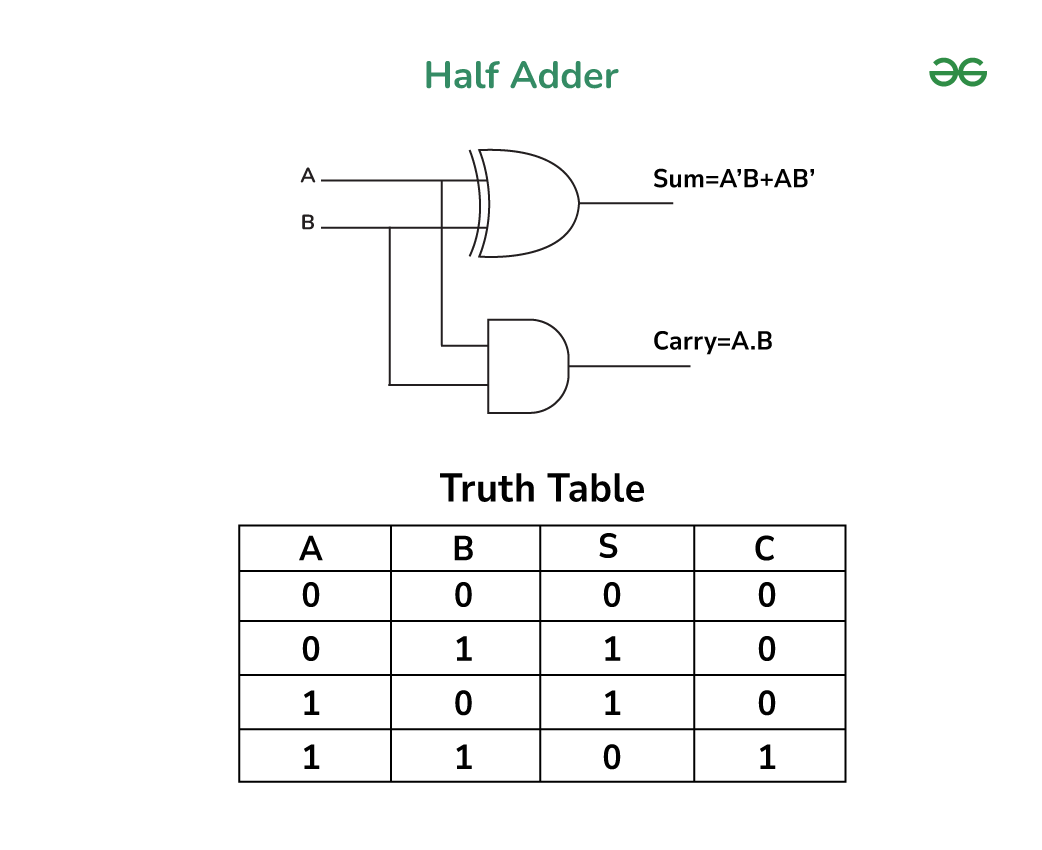
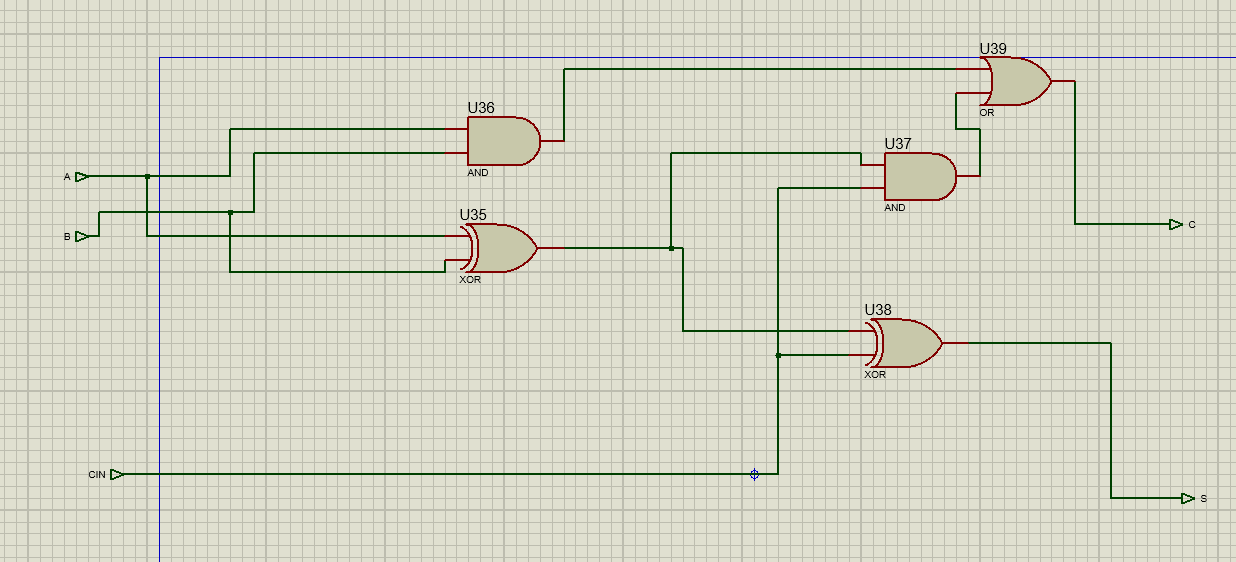


Image from : .[geeksforgeeks.org](https://www.geeksforgeeks.org/implementation-of-full-adder-using-half-adders/)

After connecting two half-adders, a circuit is created as below:



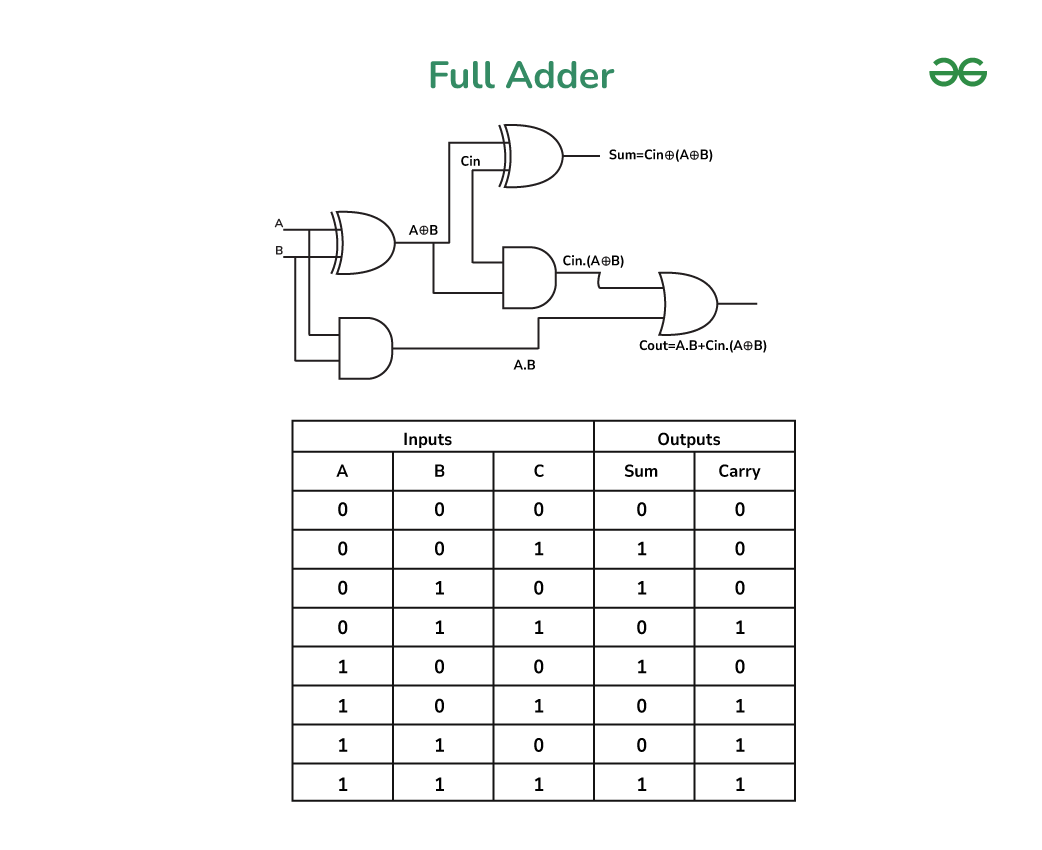
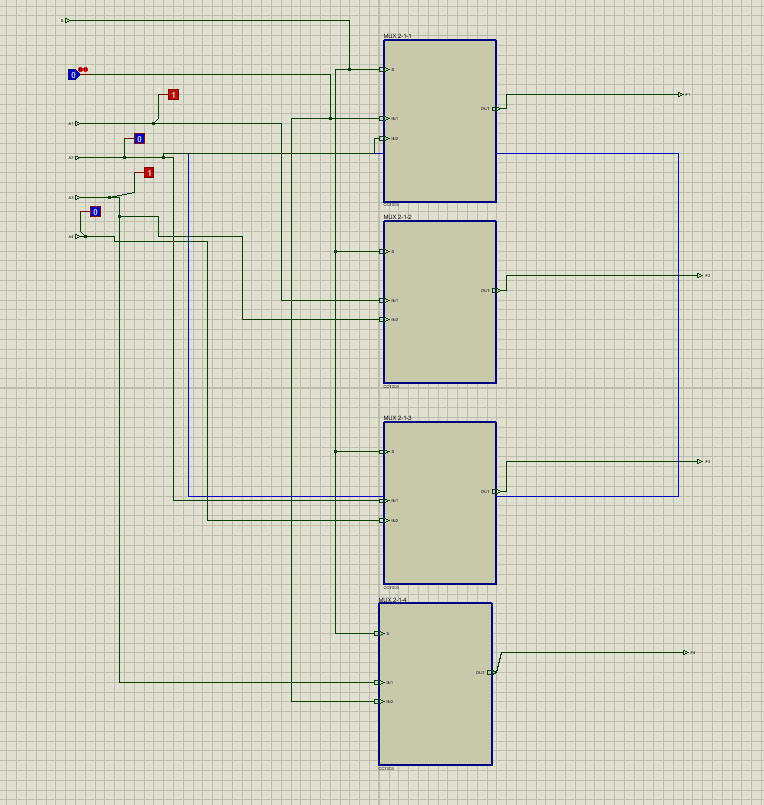


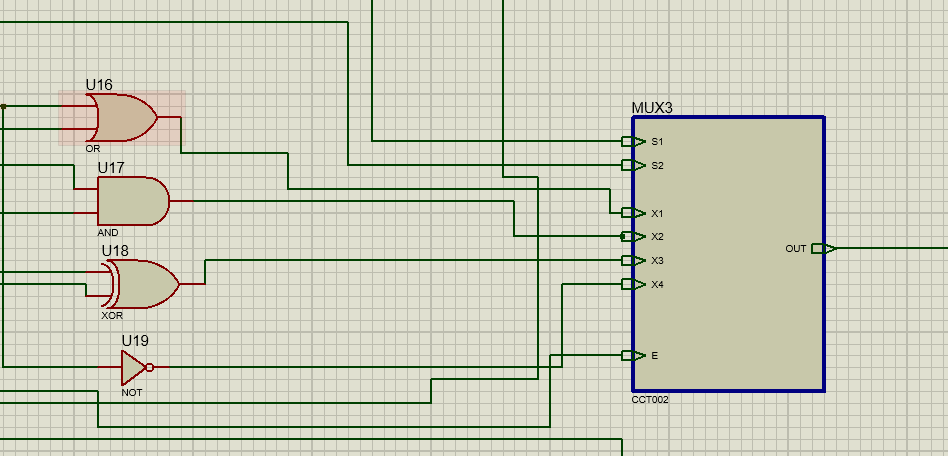
Image from : .[geeksforgeeks.org](https://www.geeksforgeeks.org/implementation-of-full-adder-using-half-adders/)

HOW TO MAKE A SHIFT CIRCUIT?

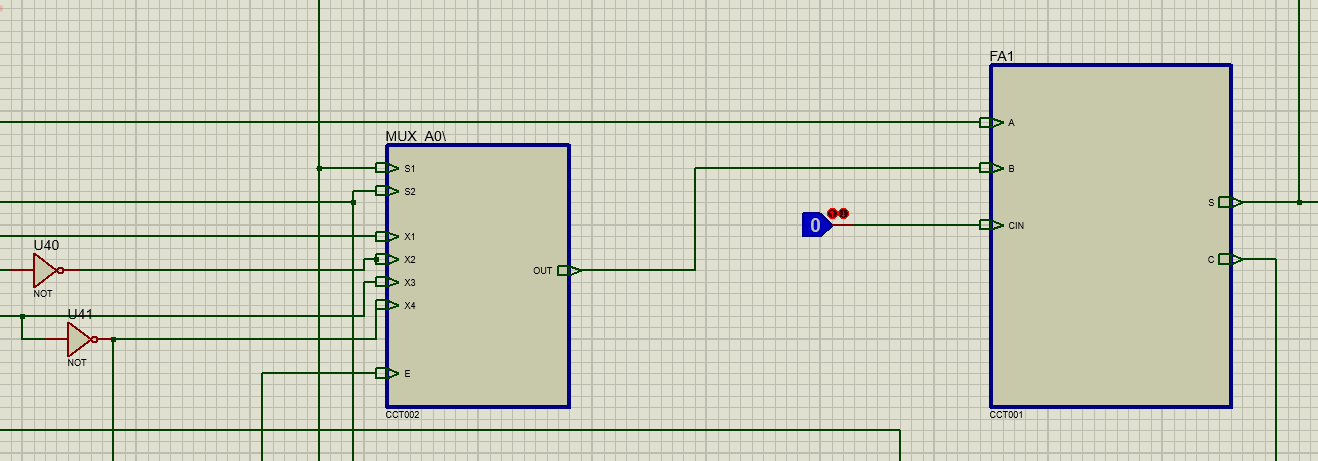
To build a shift circuit, you need a MUX and one input, which is usually 0.



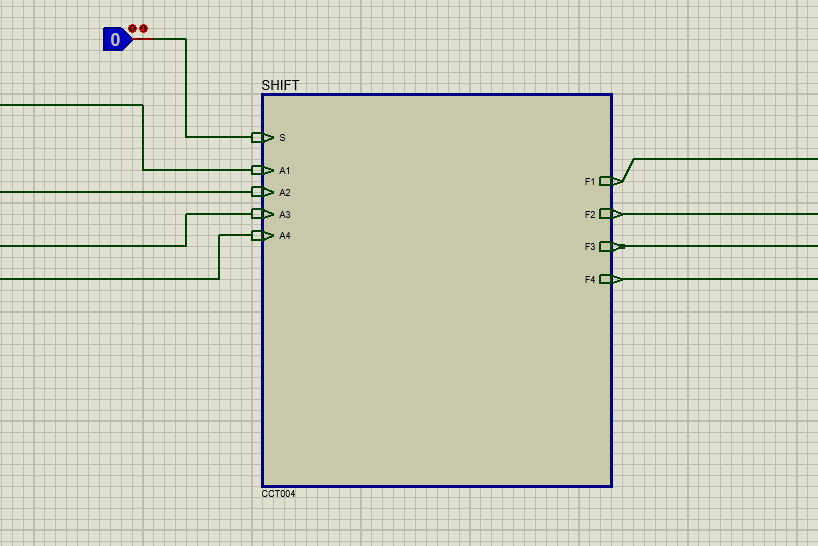
Logic unit



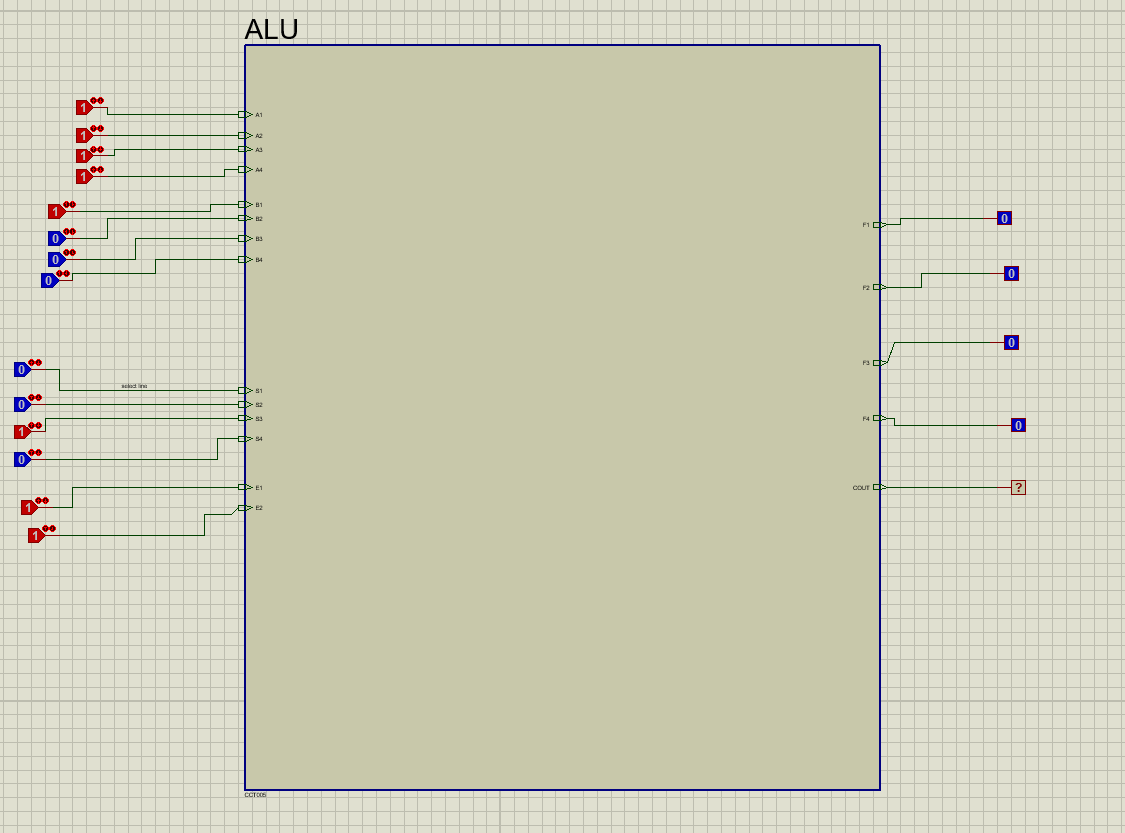
Arithmetic unit



Shift unit



By connecting the built parts, we reach the final circuit.



***INSTRUCTION TABLE***

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| E1 | E2 | S1 | S2 | S3 | S4 | OUT |
| 0 | 0 | \_ | \_ | \_ | \_ | \_ |
| 0 | 1 | \_ | \_ | \_ | \_ | \_ |
| 1 | 0 | \_ | \_ | \_ | \_ | \_ |
| 1 | 1 | \_ | \_ | \_ | \_ | \_ |
| 1 | 1 | 0 | 0 | 0 | 0 | A OR B |
| 1 | 1 | 0 | 0 | 0 | 1 | A AND B |
| 1 | 1 | 0 | 0 | 1 | 0 | A XOR B |
| 1 | 1 | 0 | 0 | 1 | 1 | A NOT |
| 1 | 1 | 0 | 1 | 0 | 0 | A ADD B |
| 1 | 1 | 0 | 1 | 0 | 1 | A SUB B |
| 1 | 1 | 0 | 1 | 1 | 0 | A SUB 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | A ADD 1 |
| 1 | 1 | 1 | 0 | \_ | \_ | A SHR |
| 1 | 1 | 1 | 1 | \_ | \_ | A SHL |